NOvA FEB
Programming Manual

2010-06-02

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Overview

The FEB utilizes registers in a 16 bit address and data space to control its functionality. One of these registers is used as a command register and the rest are used to specify details of how the FEB operates. This document describes the use of each register and is intended to be a programmer's users guide.

The details on the underlying communication protocol between the FEB and DCM are found in NOVA Document 814. This document includes the data packet structure and details on reading and writing FEB registers.

Command

Commands are written to this register to control the operation of the FEB. The command is executed immediately following the write operation. The FEB will respond to the following commands.

Reset FEB 0x1000

Put the FEB in a post configured state. This command will stop the DAQ, clear all memory and registers, restart the clock PLL, and reset communication with the DCM. It is intended that this command only be used during testing.

Start DAQ 0x1001

The Start DAQ command will enable the FEB to process and send data to the DCM. The method used to process data is set using the Mode register.

Stop DAQ 0x1002

Immediately stop the current operation, stop sending data packets to the DCM, flush all data buffers and remain idle. The FEB will complete any data packet that has been started. The FEB will always maintain communication with the DCM and send the required status packets.

Reset Current Time 0x2000

Stop the timestamp from incrementing and set its value to 0x0000 0000.

Reset USB Spy 0xF000

Reconfigure the USB Spy.

Enable USB Spy 0xF001

Enable the USB Spy.

Disable USB Spy 0xF002

Disable the USB Spy.

Set NOvA APD Readout ASIC 0x3000

Program the APD Readout ASIC with the values that are contained in the ASIC programming register.

Status

Information concerning the operation of the FEB. The definition of the bits is TBD.

Error Flag

When an error is detected it will be flagged by setting a bit in the Error Flag. When this register is read it will automatically clear all error bits. The definition of the bits is TBD.

Temperature

The Temperature register will be automatically updated at a rate of 1 Hz. Temperature data is represented by a 14-bit, two's complement word with a LSB equal to 0.03125°C

Current Time

The Current time is used to timestamp the APD data. The upper and lower registers can be used to set the current time only when the DAQ is in idle mode. The DAQ can be put into an idle mode by issuing the Stop DAQ command. The current time can be reset to 0x0000 0000 by issuing the Reset Current Time command. Only the 29 MSb can be set

DAQ Mode

Normal DSP 0x0000

This will be the normal running mode of the FEB. The FEB will digitize APD data from the Readout ASIC and process the incoming samples using DCS filtering coefficients. If the filtered data exceeds its specified threshold value the channel is marked as being triggered. A channel is in this triggered state until it falls below 1/2 the threshold value when it then enters a readout state. During the readout state it will wait to be put into the readout buffer. The readout buffer can only be written to by one channel at a time, therefore, if multiple channels enter a readout state simultaneously each channel will need to wait for its turn to be put into the buffer. The format of the resulting data packet is specified in NOVA Document 814.

Oscilloscope mode 0x1000

The FEB will operate similar to a digital storage oscilloscope. The digitized APD data from the enabled channels will be buffered in one continuous time slice. Since the buffer memory is fixed and shared between all channels the length of the time slice is determined by the number of channels that are enabled. Each sample will be sent one data packet at a time using the same format as normal DSP mode.

Memory Mode 0x2000

The FEBs output buffer is written to directly by the DCM.

Memory Loop Mode 0x2001

The FEB's output buffer is written to directly by the DCM and it continuously loops.

Channel Enable Upper/Lower

Specify what channel data will end up in the output buffer. Bit number corresponds to channel number. Set to one enables channel. This bit is used the Normal DSP and Oscilloscope DAQ mode. During other test modes this register is ignored.

Trigger threshold

32 Trigger registers correspond to channel number

ASIC Programming Register

A description of the register settings can be found in NOVA Document 4371. Writing to these registers only sets the registers internal to the FPGA. The user must issue the command to program the ASIC with the values that have been set.

Pulser Enable

The Pulser functionality is only used during debug and testing and can be left as disabled during normal operation. The FEB Pulser provides a way to synchronize the digitization of APD data with external APD light injection or charge injection into the Readout ASIC. This synchronization is required to catch the data that corresponds with an external stimulus. The Pulser Enable bits determine what part of the FEB will see the pulse. A common test preformed is to start the FEB in oscilloscope mode and begin to record the digitized data. The external pulse is then used to trigger a calibrated injection of charge. The digitized data is then read out and analyzed. The scope of the pulser is selected using the following bits.

Internal Pulse Bit 0

Triggers the output buffer to collect a new set of data. This signal is pulsed in advance of the others to provide data before signals are injected.

ASIC Testinject Bit 2

Inject charge into unmasked channels via the ASIC's internal charge injection circuit. The amount of charge and channel mask are set using the ASIC Programming registers. This method of charge injection is not intended as a calibration method.

External Pulse Bit 2

Enables the external pulse output that can be used with instruments such as oscilloscopes and pulse generators .

Pulser Periodicity

The pulse can be a single shot or periodic. When Pulser Periodicity is set to “0x0001”, the write process will cause a single pulse event. Otherwise a pulse will periodically be sent with a period of 1µs * Pulser Periodicity.

External Pulser Width

Sets the pulse width of the External pulse.

DCM Comm Test

This is a loop-back register that is only used for initial DCM testing. Data written to this register will be sent directly back to the DCM.

Firmware Limitations

Some of the functionality described here is currently under development. It is however intended to have everything in this document implemented for use in the IPND.

Memory Modes

The Memory test modes are not implemented.

DCM Communication

The DCM communication has been tested by putting the FEB in a loop-back test mode and the FEB and DCM have been verified to understand each others 8B10B basic communication. However, the FEB can not currently encode or decode the packet structure as defined in NOVA Document 814

Address	Contents (Valid:Bits)	Direction	Default Value

FEB Command and Status Registers			
0x0001	Command(15:0)	W	
0x0002	Status(15:0)	R	
0x0003	Error Flag(15:0)	R	
0x0010	Current_Time_L(15:2)	R/W	0x0000
0x0011	Current_Time_U(15:0)	R/W	0x0000
0x0012	reserved		
0x0013	reserved		
0x0020	Temperature(13:0)	R/W	0x000
0x0021	Temperature_Timestamp_L(15:0)	R/W	0x0000
0x0022	Temperature_Timestamp_U(15:0)	R/W	0x0000
Registers to control the FEB modes of operaton			
0x1000	DAQ Mode(15:0)	R/W	0x0000
0x1001	Channel Enable Upper(15:0)	R/W	0x0000
0x1002	Channel Enable Lower(15:0)	R/W	0x0000
Trigger threshold			
0x2000	Trigger threshold Ch0(12:0)	R/W	0x000
0x2001	Trigger threshold Ch1(12:0)	R/W	0x000
...	...		
0x201F	Trigger threshold Ch31(12:0)	R/W	0x000
TECC Status and Control			
0x3000	Setpoint(11:0)	W	0x000
0x3001	Setpoint_Timestamp_L(15:0)	R	0x0000
0x3002	Setpoint_Timestamp_U(15:0)	R	0x0000
0x3010	Drive Monitor(11:0)	R/W	0x000
0x3011	Drive Monitor_Timestamp_L(15:0)	R	0x0000
0x3012	Drive Monitor_Timestamp_U(15:0)	R	0x0000
0x3020	Temp Monitor(11:0)	R/W	0x000
0x3021	Temp Monitor_Timestamp_L(15:0)	R	0x0000
0x3022	Temp Monitor_Timestamp_U(15:0)	R	0x0000
ASIC Programming Registers			
0x4040	Spare(0:5)	R/W	
0x4041	VtSel(0:2)	R/W	
0x4042	RefSel(0:3)	R/W	
0x4043	ISel(0:2)	R/W	
0x4044	BWSel(0:3)	R/W	
0x4045	GSel(0:2)	R/W	
0x4046	TfSel(0:2)	R/W	
0x4047	Mux2to1(0)	R/W	
0x4048	Mux8to1(0)	R/W	
0x4000	Offs0(0:4) (channel 0)	R/W	
0x4020	Mask0 (0)(channel 0)	R/W	
0x4001	Offs1(0:4) (channel 1)	R/W	
0x4021	Mask1(0) (channel 1)	R/W	
0x4002	Offs1(0:4) (channel 2)	R/W	
0x4022	Mask1(0) (channel 2)	R/W	

...	...		
...	...		
0x401f	Offs31(0:4) (channel 31)	R/W	
0x403f	Mask31 (channel 31)	R/W	
DSP Filter coefficients			
0x8xxx	TBD	R/W	
0x9xxx	TBD	R/W	
0xAxxx	TBD	R/W	
Registers only used during testing and debugging			
0xF000	Pulser Enable(15:0)	R/W	0x0000
0xF001	Pulser Periodicity(15:0)	R/W	0x0000
0xF002	Pulser Width(15:0)	R/W	0x0000
0xF100	DCM Comm Test	R/W	
Reserved Addresses			
0xE005	DCM Emulator internal		